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[57] **ABSTRACT**

This semiconductor circuit includes a plurality of memory cell arrays arranged mutually adjacent in one direction, a plurality of first selection/sense amplifier circuits provided in the respective regions between mutually adjacent pairs of these memory cell arrays and make access to one of alternately defined odd-numbered or even-numbered memory cell trains in the order of arrangement, two units of second selection/sense amplifier circuits arranged on the outside of the memory cell arrays on both ends of the arrangement of the plurality of memory cell arrays and make access to one of the designated odd-numbered or even-numbered memory cell trains of the memory cell arrays on both ends, a plurality of data buses corresponding to the respective bits of data transferred in bit parallel between an external circuit, and a plurality of input and output switching circuits arranged and connected in one-to-one correspondence to the respective first and second selection/-sense amplifier circuits connected to the plurality of data buses so as to have an equal number of memory cell trains capable of transferring data with these data buses, and a plurality of input and output switching circuits which transfer data with the first and the second selection/sense amplifier circuits in one-to-one correspondence.

3 Claims, 4 Drawing Sheets

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